

Effects of via-conductor geometry in the electromigration failure of Al:Cu wires

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ABSTRACT

Electromigration (EM) experiments conducted using two types of via/plug to conductor alignment indicate a geometrical dependence of electromigration failure in Al:Cu conductors. The resistance vs time curves show distinctive steps when the alignment is parallel. This is explained by a successive loss of conductivity trough the plug due to void formation. In the perpendicular via/conductor arrangement, resistance increases by smaller and closely spaced steps. EM experiments without vias, found that the conductor life under stress increases by at least an order of magnitude. Kinetic studies at four temperatures between 180-240 C found activation energies to be $1.0 \pm 0.1 \text{ eV}$.

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Outline

- Experimental set-up/Background
- Resistance Vs. time
 - Conductor orientation dependence
 - Results without vias
- EBIC imaging
- Activation energy determination
- Cross-sectional images
- Some of the problems, difficulties...
- Summary/Conclusions

Motivation/Purpose

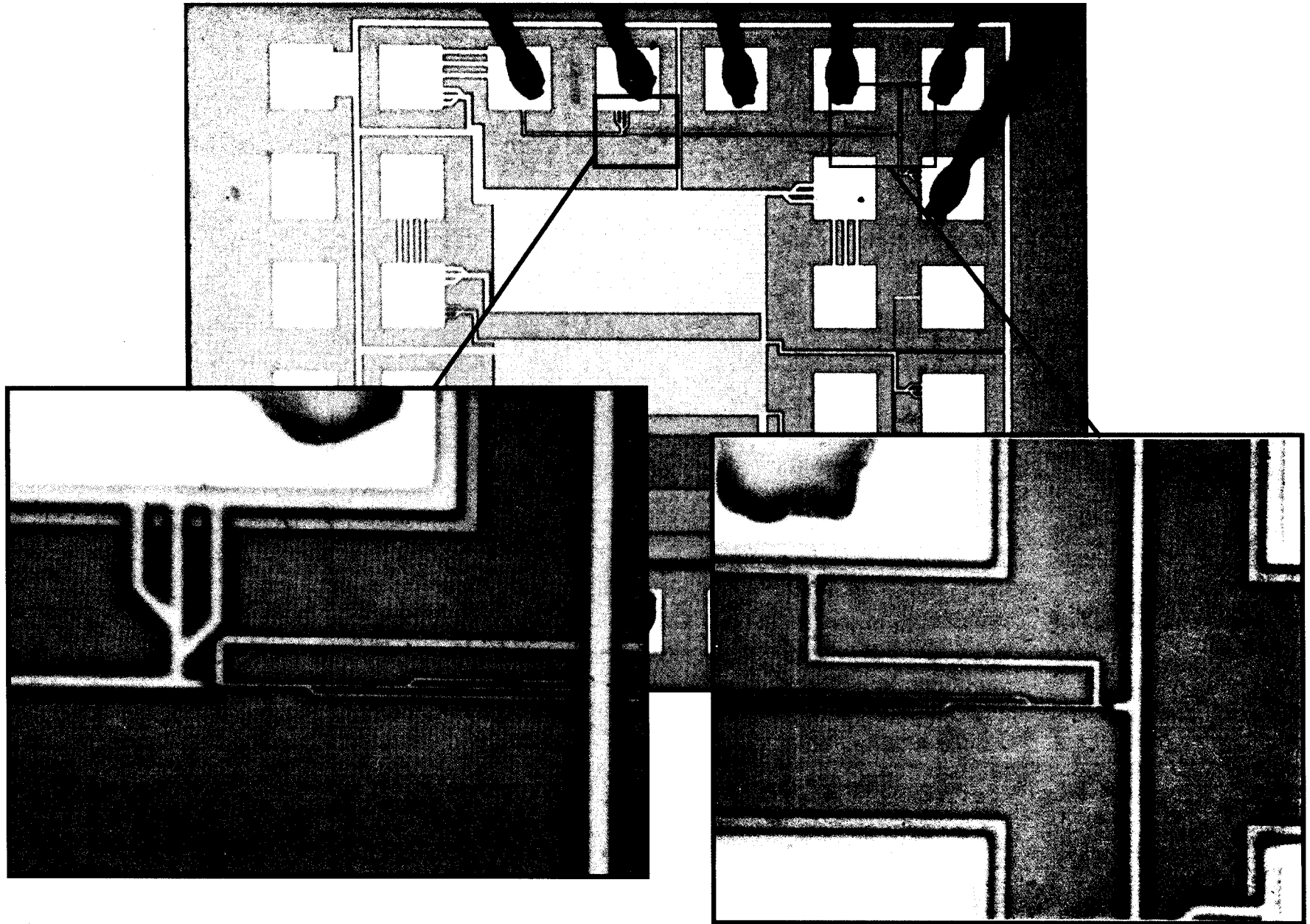
- As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity.
- These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits. EM failure models for Al-Cu metallization at tungsten plug contact/via areas are examined in this work.
- In particular, we examine changes induced solely by the geometry of the plug via conductor arrangement.
- Performing these experiments at various temperatures also allowed determination of the temperature dependence of this geometrical dependence.

Experimental details

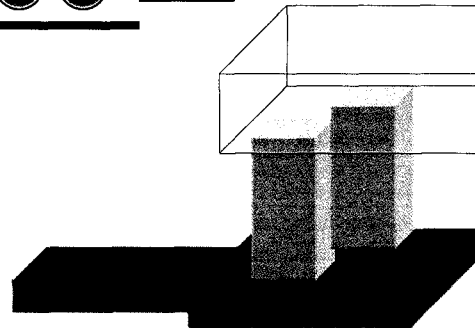
- Four probe measurements at constant current
- Two via geometries in 2 layer metallization test structures*
 - two structures tested at one time
 - different vias are made to fail by reversing current direction
 - experiments were also performed with no vias
- Test structure is Al:Cu (2% Cu). Diffusion barrier - passivation layer - tungsten plugs - Conductor critical dimensions: 0.67 microns deep by 0.67 microns wide - Bamboo structure (grain sizes ~ 1 micron)
- Resistance is measured and acquired digitally every 30 minutes
- Measurements at four (4) temperatures: 180, 200, 220 and 240°C
- Currents used are 8, 10 20 mA (corresponding to current densities of $1.6 \times 10^6/\text{cm}^2$, $2 \times 10^6/\text{cm}^2$ and $4 \times 10^6/\text{cm}^2$)
 - R vs T at low currents was measured to detect possible Joule heating at high current densities.
- Measurements were performed in air ant at 1 atmosphere
- EBIC (Electron Beam Induced Conductivity) to isolate failure sites was performed at 10 KeV

*Fabricated at IDT (Integrated Device Technology, Inc.) at their San Jose foundry (now closed)

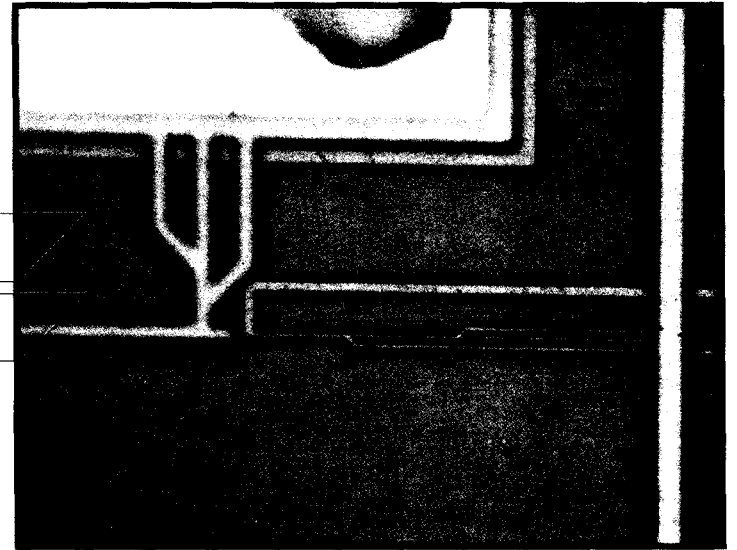
Test structure for Al:Cu electromigration testing



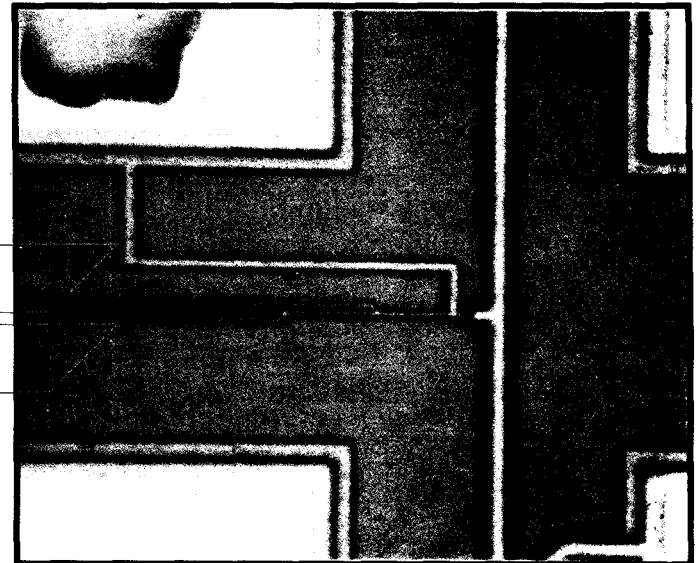
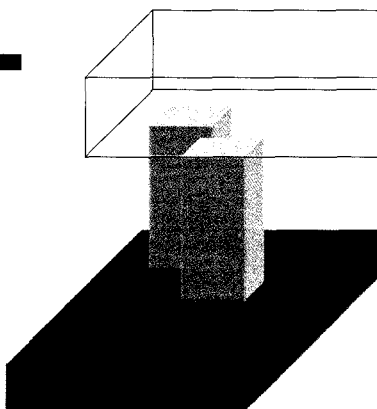
Parallel or co-linear geometry



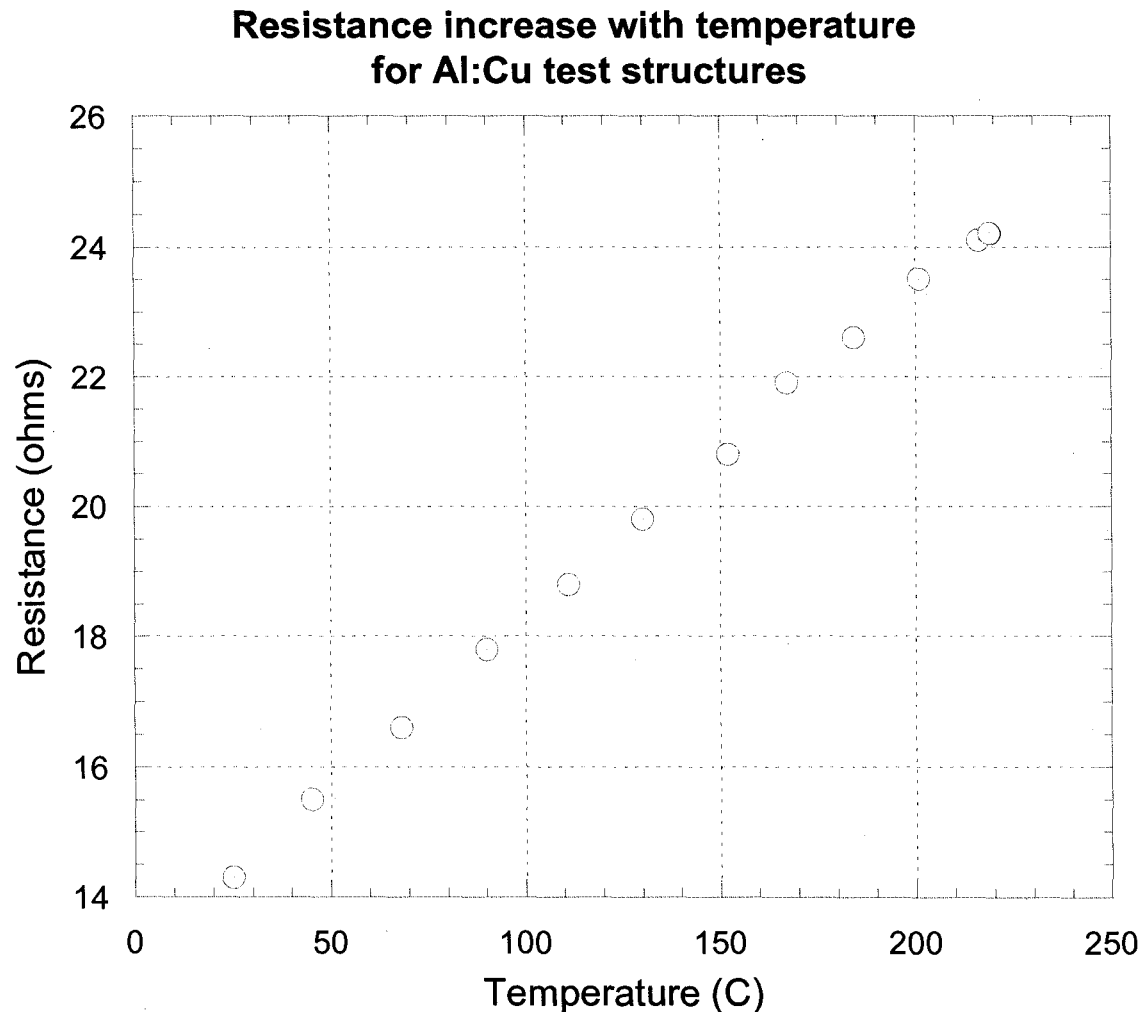
Aluminum:Cu line



Perpendicular geometry

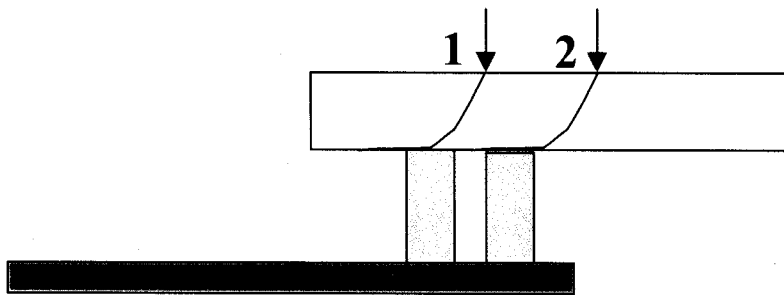


Joule heating measurements for Al:Cu test structures:

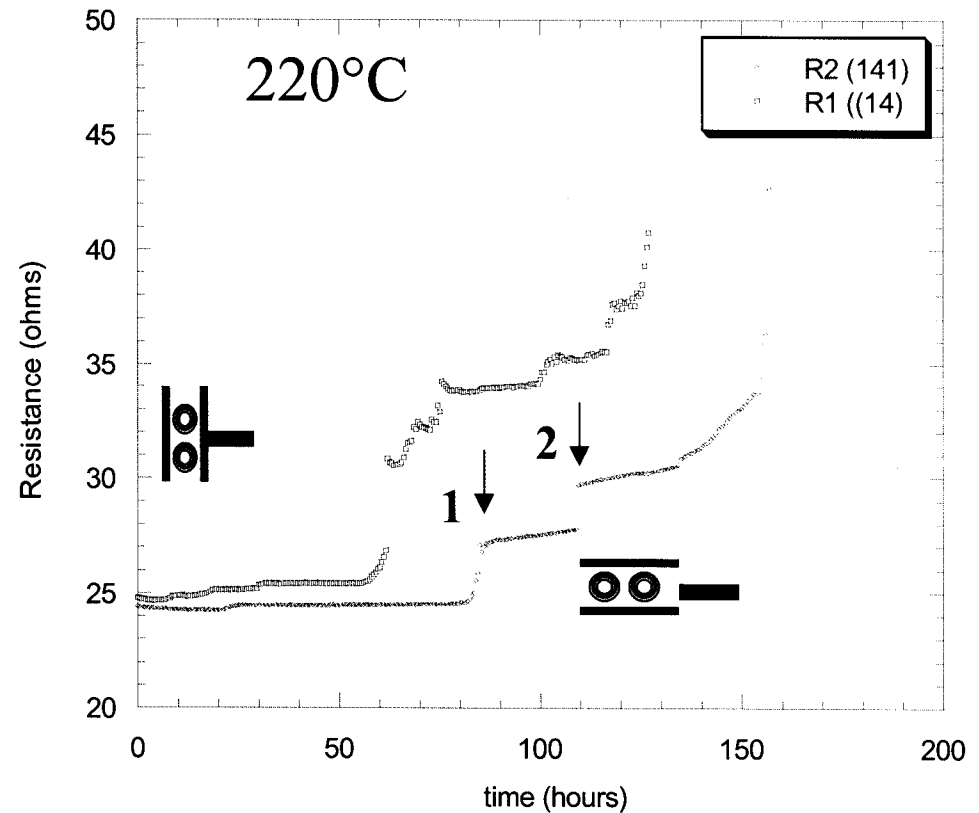


Measurements performed as structures are heated at very low current densities (current of 0.05 mA) show Joule heating of 0.05 ohms /degree C. Current density is then increased to test stress current (20 or 10 mA). No significant increase in resistance is observed at beginning of measurement.

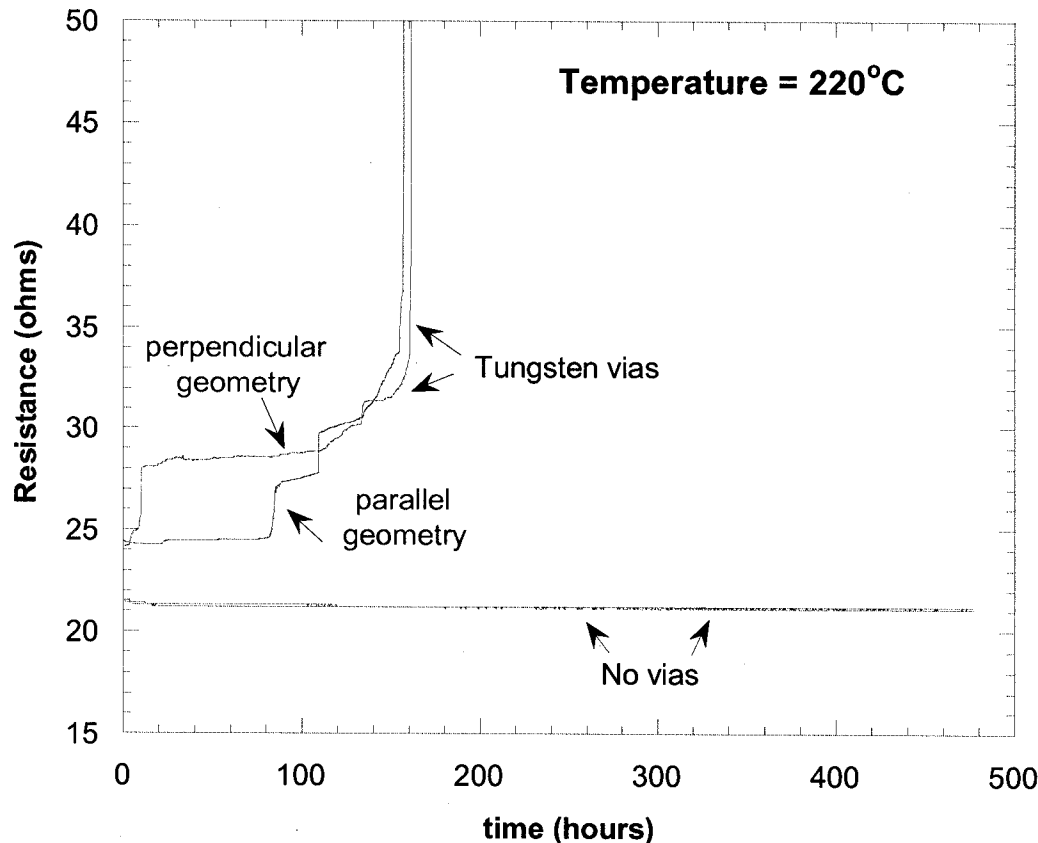
Colinear conductor geometry shows well defined
“steps in the Resistance vs. time curves



Proposed mechanism to explain
“steps” in colinear geometry.
Progressive void formation at each
plug/conductor interface could
explain measured resistance data.



Dramatic differences in degradation seen in tests with and without vias (1 and 2 layer metallization)



This observation can be explained by the absence of flux divergence in the no-via 1 layer structure. Previous studies have shown that the interface between the Al conductor and the refractory metal (W plug) is most vulnerable to voiding. This is due to the discontinuity in the flux of electromigrating Al atoms.

The rate of void formation is controlled by the Al drift velocity:

$$V_d = D_i / kT e Z_i^* \rho j$$

where: D_i is the diffusion coefficient of Aluminum
 j is the current density, r is the resistivity (of Al),
and eZ_i^* is the effective electromigration charge

EBIC has shown to be a very useful tool to identify point of failure

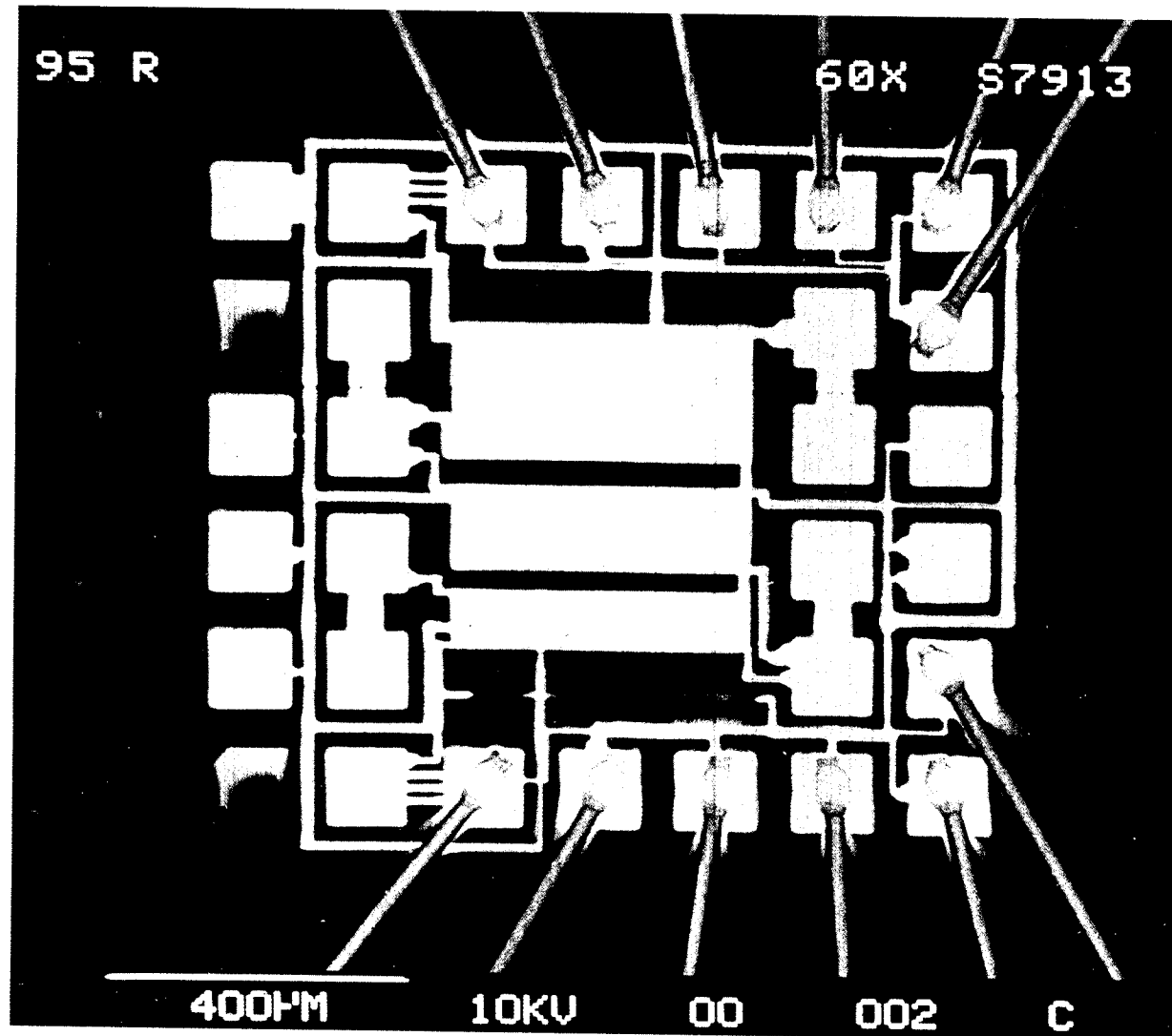
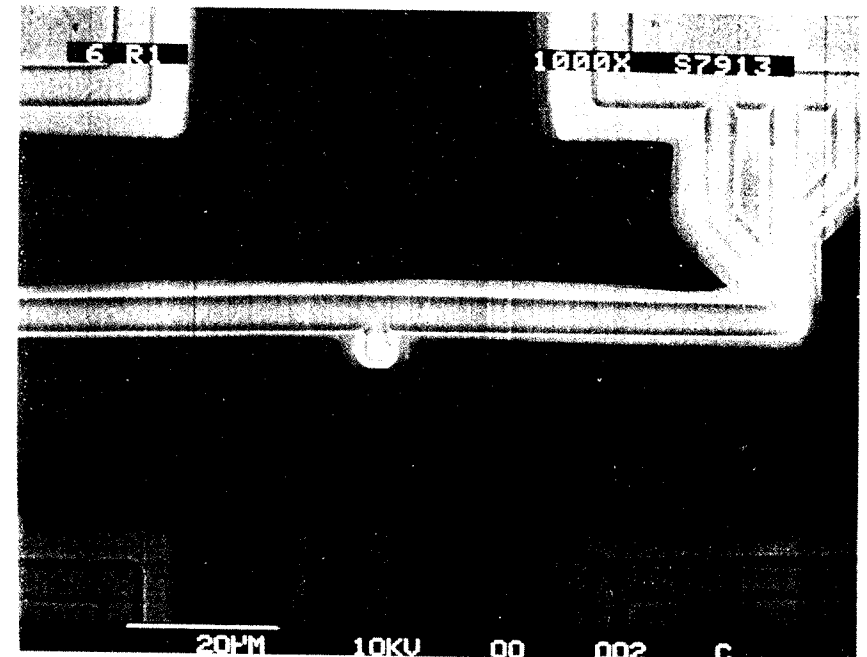
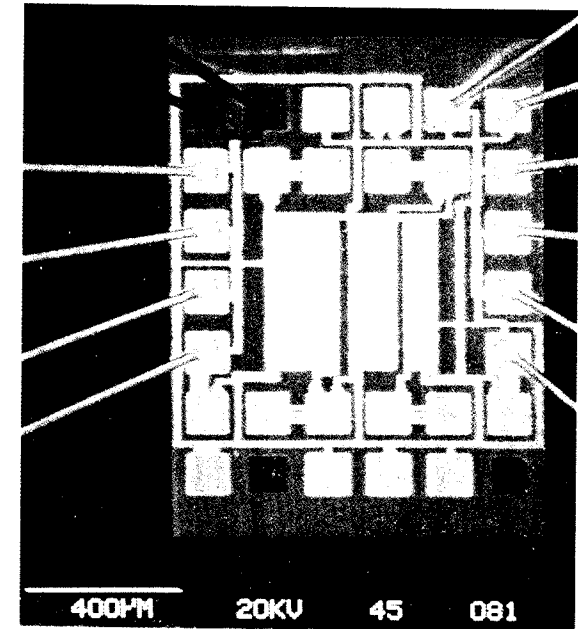
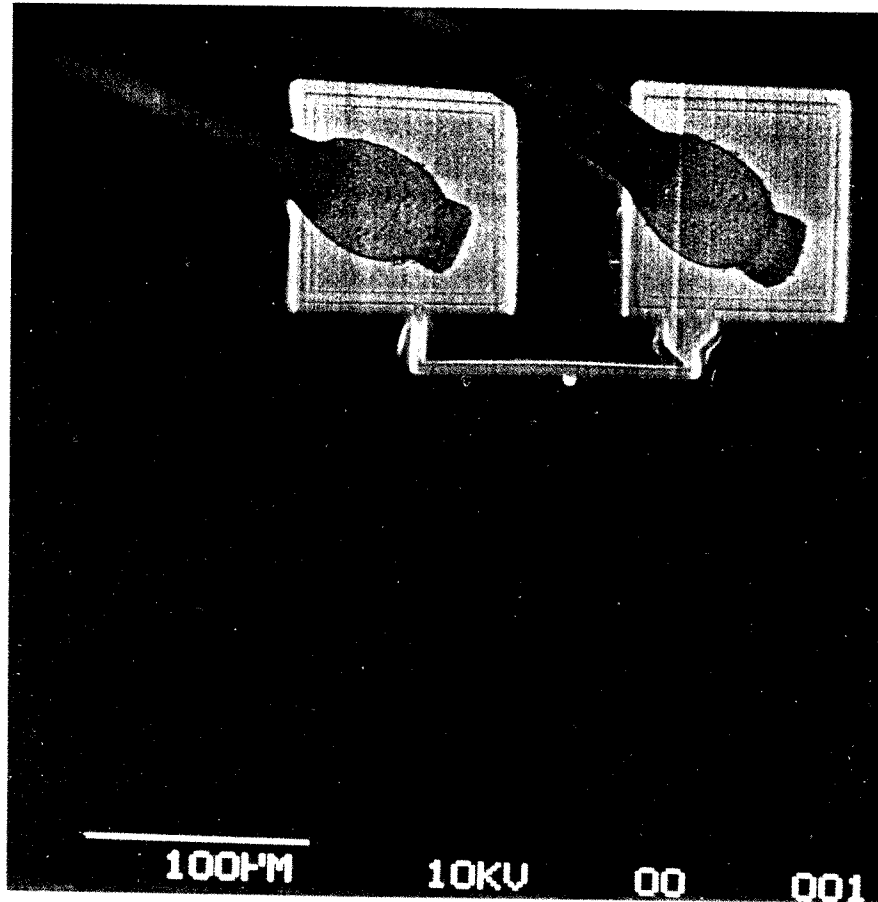


Image shows EBIC contrast when there are no open conductors.

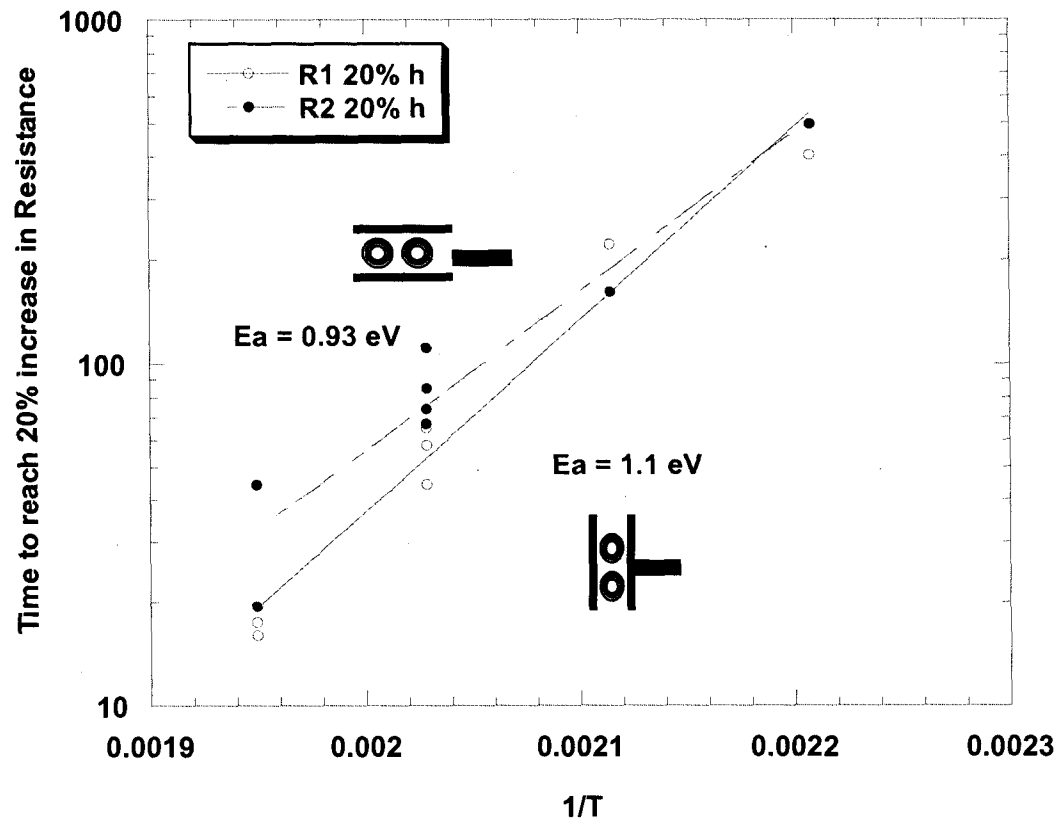
Failure point cannot be seen in plan-view (top) imaging even for an open circuit failure after electromigration testing.

EBIC analysis of open circuit structure after electromigration testing at 220 C



Connections were reversed to ensure that failure is only at one of the two vias

Al:Cu activation energy for electromigration:



Similar activation energies were obtained for the perpendicular and colinear geometries, however, our measurements show that perpendicular vias have a higher probability of failing sooner. This is reflected in a different (smaller) pre-exponential factor in the Arrhenius curve.

Fit with Black's equation,

$$t = A i^{-n} e^{E_a/kT}$$

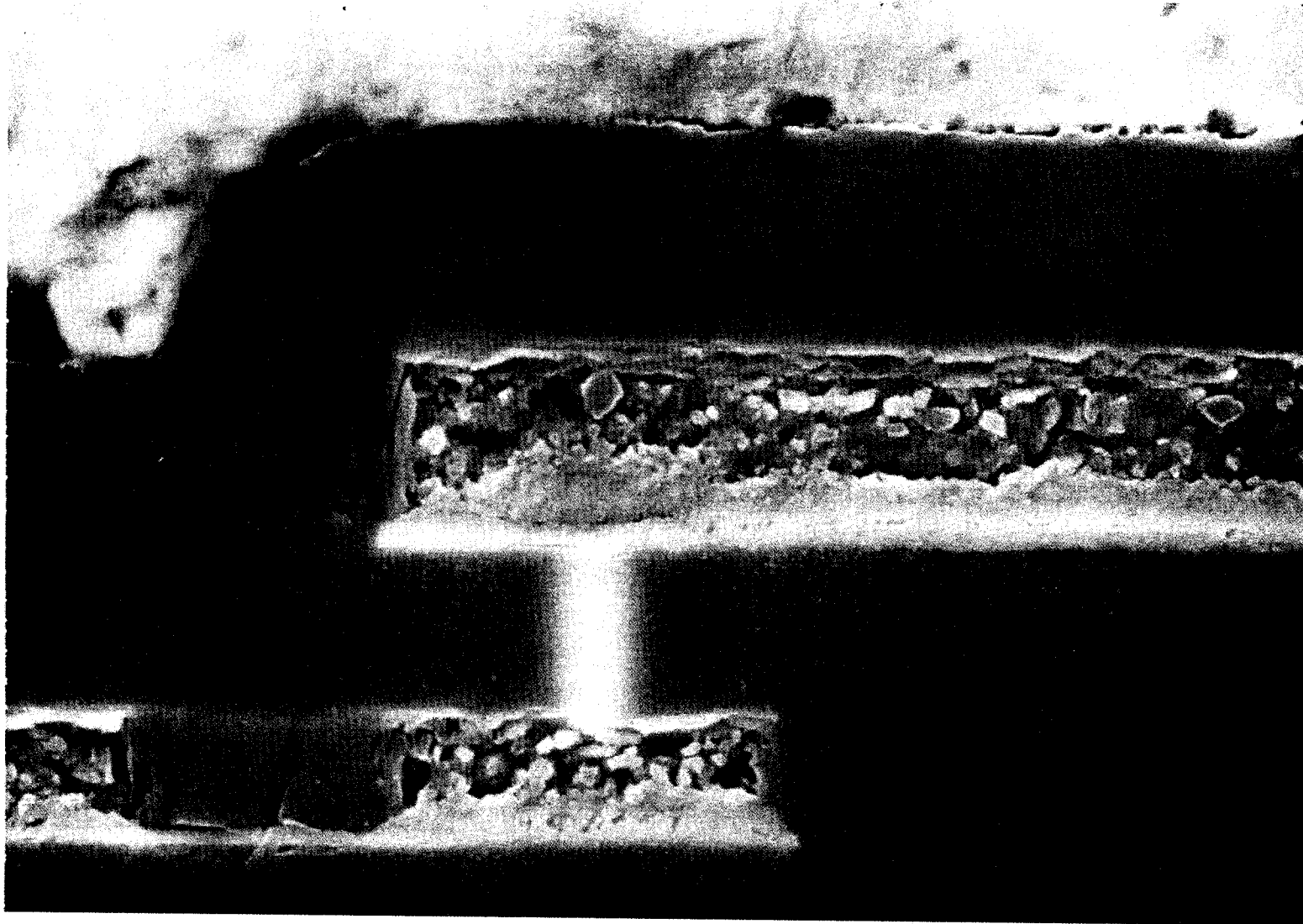
t is time to reach failure (20% degradation)

i is current density

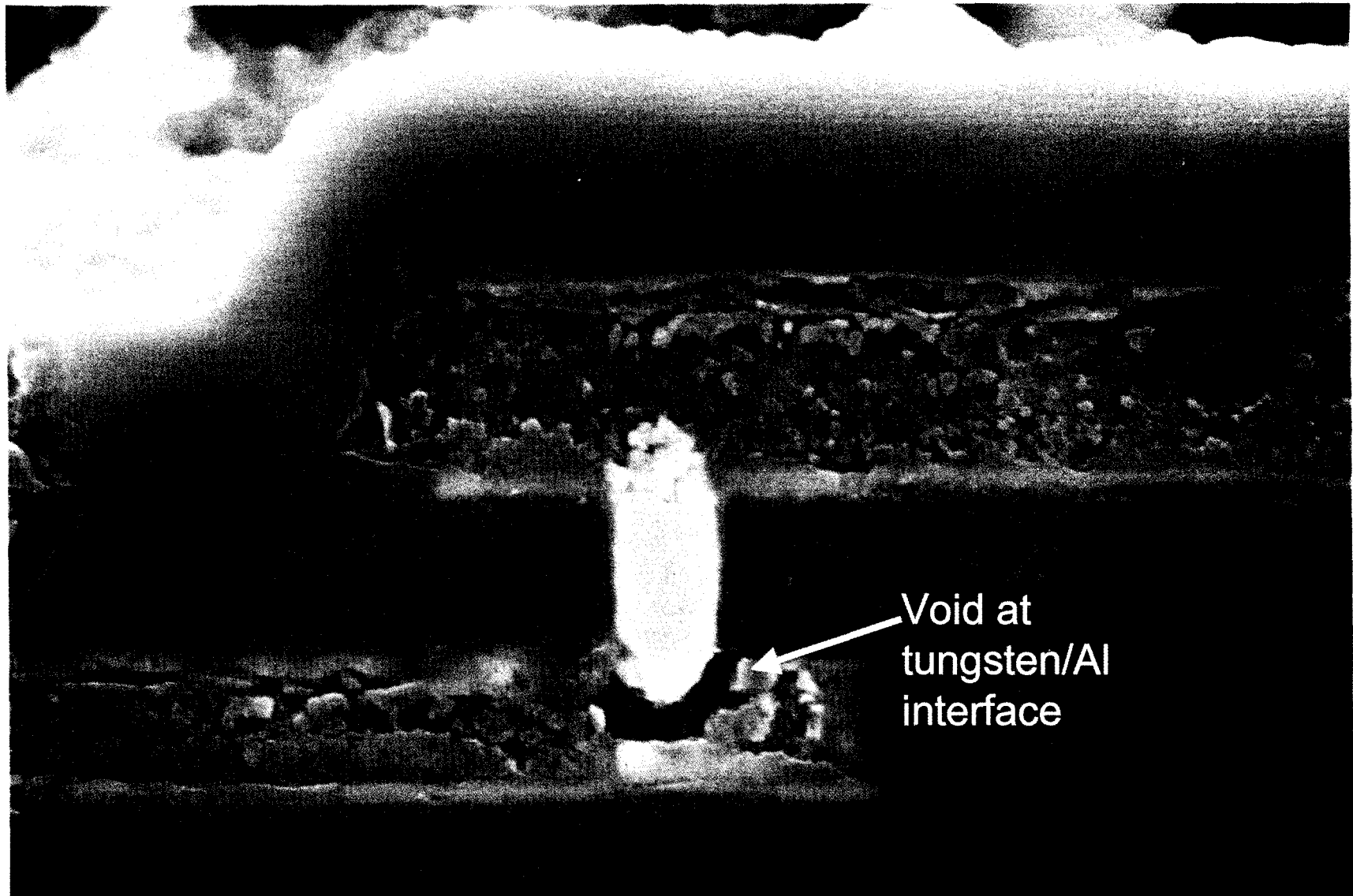
k is Boltzman's constant

Ea is activation energy (in eV)

T is temperature



Cross sectional SEM image of a “good” structure prior to EM testing, which shows one of the Tungsten plugs.



Void at
tungsten/Al
interface

Cross-sectional SEM image of voided area at Tungsten/Al:Cu interface. Void was formed from electromigration testing at 240 C and structure failed catastrophically (open circuit).

Summary of data for Al:Cu electromigration experiments – black and blue indicates measurement done in pairs. R1 is connected so perpendicular via fails, R2 is connected to fail with parallel via.

Sample #	Via failure = or \perp	Current (mA)	Current density (A/cm ²)	T (C)	Initial R at test T	Time to degrade 10%	Time to degrade 20%	Time 100% failure (open)	Comments	Failure mode
43 (Greg)	R to L	8	1.6 x 10 ⁶	220	22.2	65 h	80 h			
117 (Greg)	L to R	8	"	220	21.9	> 90 h	> 90 h		Some degrad.	
150	R to L	10	2 x 10 ⁶	220	24	34 h	35 h		In Series	
117	L to R	10		220	23	> 70 h	> 70 h		No degrad.	
92	none	20	4 x 10 ⁶	220	21.5	> 500 h	> 500 h	No R change	No via	ESD zapped
131	none	20	"	220	21.6	> 500 h	> 500 h	No R increase	No via	ESD zapped
45 (R1)	\perp	10 and 20	2 and 4	220	23.1	50 h (10mA)	58 h	315 h	EBIC (Ron)	Via failure
58 (R2)	=	10 and 20	X 10 ⁶	220	22.7	80 h (10mA)	85 h	362 h		
14 (R1)	\perp	20	4 x 10 ⁶	220	24.8	63 h	65 h	127 h	In ESD bag	Via open
141 (R2)	=	20	"	220	24.4	110 h	111 h	157 h	In ESD bag	Via open
33 (R1)	\perp	20	"	240	25.1	8.5 h	17.5	37.5 h	In ESD box	Via open
150 (R2)	=	20	"	240	26.4	23.5 h	44.5 h	57.5 h	In ESD box	Via open
31 (R1)	\perp	20	"	200	23.7	105.5 h	222 h	347 h	In ESD box	Via open
297 (R2)	=	20	"	200	23.8	28 h	162 h	290 h	In ESD box	Via open
180 (R1)	\perp	20	"	180	23.2	43 h	403 h	663 h	In ESD box	Via open
185 (R2)	=	20	"	180	22.7	290 h	497 h	773 h	In ESD box	Via open
6 (R1)	\perp	20	"	240	25.3	12.7 h	16 h	47	In ESD box	Via open
35 (R2)	=	20	"	240	25.1	6.4 h	19.5 h	48 h	In ESD box	Via open
95 (R1)	\perp	20	"	200	24.5	14.4 h	14.4 h	377 h	In ESD box	Both to 35 Ohms
283 (R2)	=	20	"	200	23.5	70 h	70 h	256 h	In ESD box	(not open)
63 (R1)	\perp	20	"	220	24.0	10 h	58 h	161 h	In ESD bag	Open circuit
326 (R2)	=	20	"	220	24.7	31 h	74 h	108 h	In ESD box	Open circuit
262 (R1)	\perp	20	"	220	24.3	15.7	44.5	103	In ESD box	40 ohms
284 (R2)	=	20	"	220	24.2	10	67	103.5	In ESD box	40 ohms
44 (R1)	\perp	10	2 x 10 ⁶	240	24.7	29	222	325	In ESD box	open
158 (R2)	=	10	"	240	25.3	32	179	413	In ESD box	open

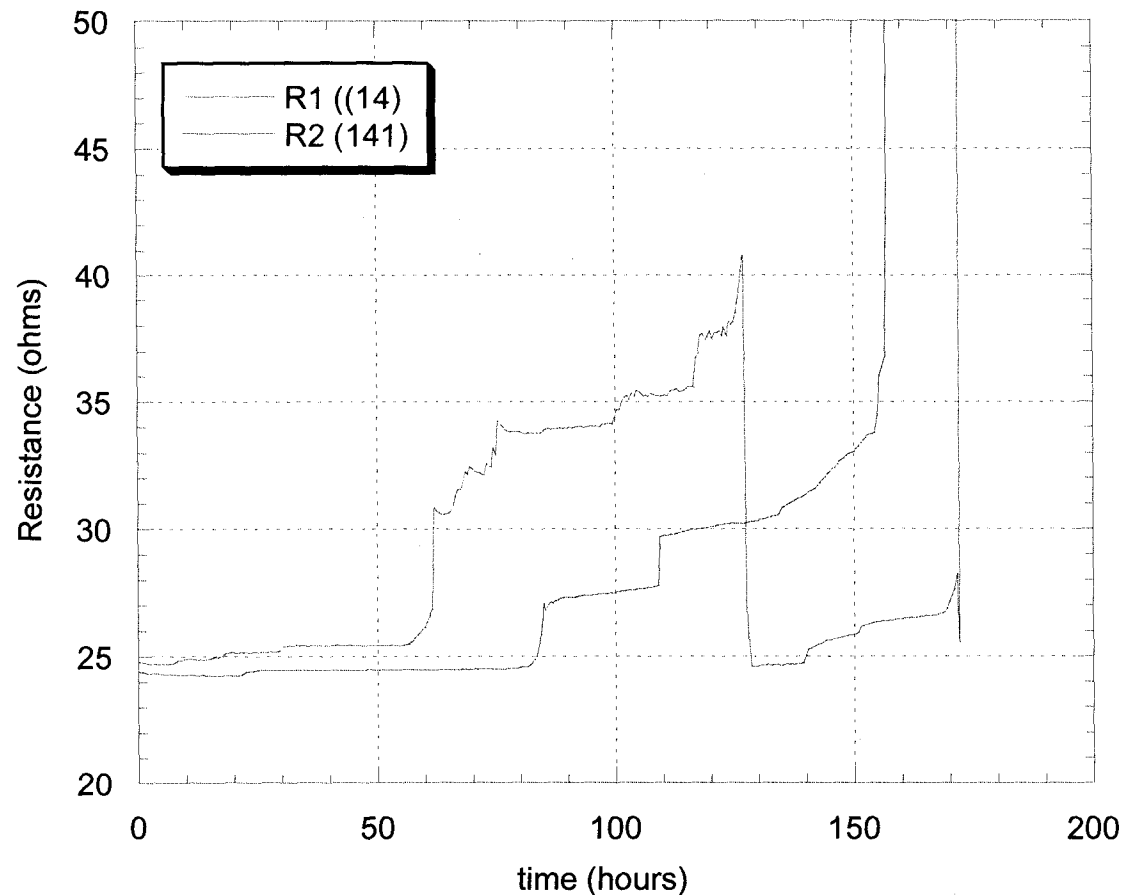
Problems (1): High ESD (electrostatic discharge) sensitivity.
Damage often seen in dry winter days



Solution:

1. Use appropriate ESD precautions during test structure handling (according to the JPL Standard for ESD Control, ~~found in D-1348 Rev. D)~~^e
2. Store structures in ESD bags or boxes in between tests or after testing and prior to cross-sectioning

Problem (2): Ultrahigh current densities in thinning areas can cause arching with localized melting of metals and partial structure “repair”. This is undesirable for cross-sectional studies since this process might mask “real” (meaning electromigration induced) degradation mechanism.



Curve for R1 (red) shows a case of localized metallization “repair” due to melting of metals at ultra-high current densities after Al conductor thinning due to electromigration induced voiding.

Test can be stopped earlier, before circuit is completely open.

Summary of Experimental observations

- We find sharp steps in the Resistance vs time curves (for the colinear geometry)
- Times to failure (or 20% degradation) have the expected Arrhenius dependence
- Activation energies obtained from Arrhenius plots are 1 eV - high for Al conductors. Failure is through grain boundary diffusion
- EBIC (electron beam induced conductivity) is a useful technique to locate failure, but it works best if line is open.
- Colinear (parallel) geometry is more likely to fail after structures with perpendicular geometry under the same conditions (as seen in 7 out of 8 test pairs)
- Earlier degradation does not necessarily mean early catastrophic failure